ADC Technologies related to BRIAR

Currently, ADC is equipped with core technologies as follows:

1. Unsupervised Learning based Bio-inspired Visual system

a) Bio-inspired Extended Visual Pathway (EViP) software, which integrates a saccadic eye movement emulator with an advanced model of the human visual pathway, to enable real-time processing for the detection and recognition of single or multiple objects, given inputs that are:

- partial-view or full-view
- low resolution or "noisy"
- incomplete or "collage" style
- sketches of actual objects.

b) MegaFace testing (based on one sample training on an object like a human visual system)

Benchmark tests show the EViP **exceeds human visual performance** at correctly picking out single images in a 10,000-image database in Rank 1 recognition (i.e., "best match") tests.

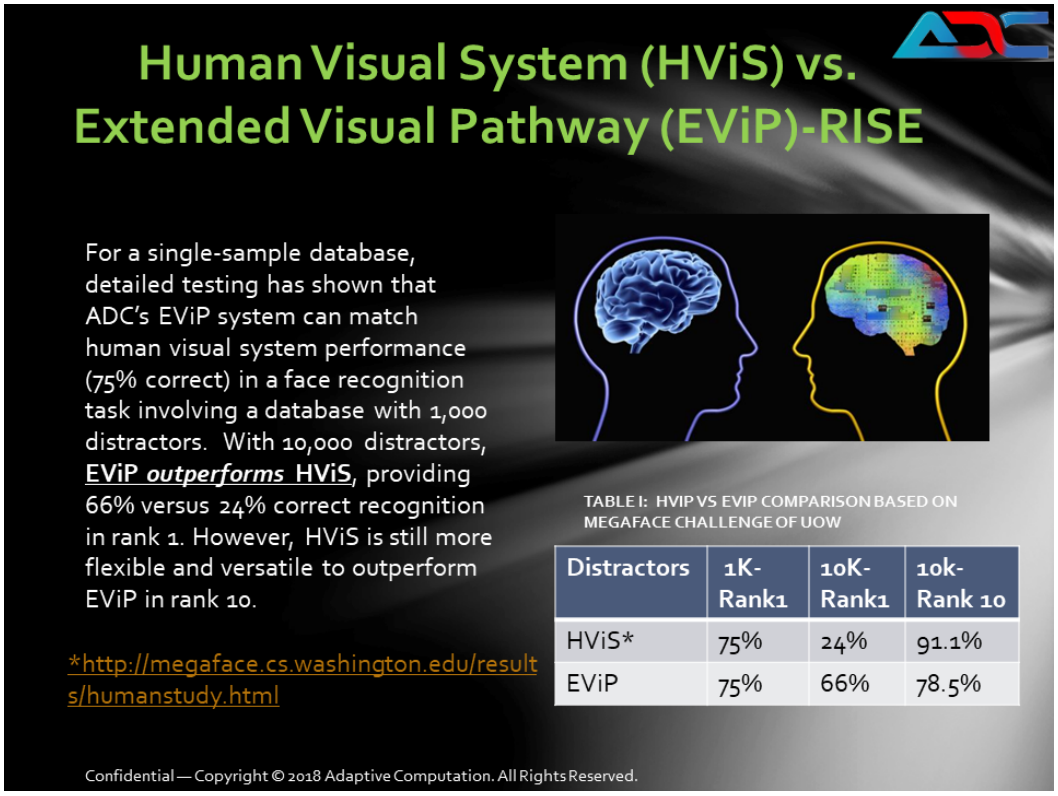

Figure 1. EViP vs Human Visual System (HViS) based on a single glance on an object

c) Near IR Statistical Study

We tested our system with a Near IR Image Face data set from the University of Notre Dame [1] with 22,266 faces from 559 subjects shown in Table I. We trained the system with 559 single images (single glance on an object)—a front face shot of each subject. The remaining images were used to test the system's ability to correctly identify them. The results for "Rank 1" Identification Task ("best guess at who this is") is 91.7% correct. This result is equivalent to our study for NIST Face database for day light object.

Table I: EViP performance based on single glance on an object (one sample training on an object like human visual system)

	Data samples	Comments
Training	559	Each sample per subject
Test	22,226	On average, it is 40 samples per subject in different pose, condition etc.
Performance	91.8% correct in rank 1	Rank 1 is the best choice.

The Extended Visual Pathway (EViP) is firstly introduced and published the initial work in the Handbook of Pattern Recognition, 2011[2] . ADC owns four patents [3,4,5,6] including an international patent. This technology is a novel and powerful bio-inspired technique – developed by the PI, Dr. Tuan A. Duong, who was with NASA's Jet Propulsion Laboratory (JPL) for 26-years of research in neural networks.

2. Supervised Learning- a Dynamic Self-Evolving Learning Architecture

Non-competitive Supervised learning (NSL) can learn all the dynamic changes of objects that are supplied by EViP and serve as long-term memory in the brain-like system. The uniqueness of the NSL is learning its specific object itself, without competing against other objects, to gain the speed and easy learning convergence. ADC is equipped with a technique to alleviate the expected high false alarms from other objects due to this learning style.
The obstacles for supervised learning like BackProp are how to define system architecture (e.g., how many hidden layers, how many units in each layer etc.), learning rate sensitivity (due to multiple identical learning attractors that exist in this architecture), accommodating new data with a learned system (it may require learning from scratch again). These obstacles must be clear

[1] http://www3.nd.edu/ cvrl/CVRL/Data Sets.html

[2] Tuan A. Duong, Vu A. Duong and Allen R. Stubberud, "Shape and Color Features for Object Recognition Search,", Handbook of Pattern Recognition and Computer Vision, Chap. 1.5, Ed. C.H. Chen, 4th Edition by World Scientific Publishing Co. Pte. Ltd, Jan 2010.

[3] US patent, "Systems and Methods for Object Recognition Based on Human Visual Pathway," Tuan A Duong, Patent No. 14/986,057, Issue Date November 20, 2018.

[4] US Patent No. 9,846,808, "Image Integration Search Based on Human Visual Pathway Model," Tuan A Duong, Issued December 19, 2017.

[5] International patent WO 2017/116916 A1, " Image Integration Search Based on Human Visual Pathway Model," Issued July 06, 2017.

[6] US patent, "Image Integration Search Based on Human Visual Pathway Model," Tuan A Duong, Patent No. 10289927, Issue Date May 14, 2019.

for autonomous learning system. Deep learning has found its own architecture set and used as a blanket one for most of system; hence it is not an optimal selection set.
Cascade Error Projection (CEP) [2,7,8] developed by the PI for NASA mission is a more versatile approach where data-dependent self-evolving architecture is introduced (It is learning from cascade correlation from Scott Fahlman from CMU), non-sensitivity learning rate (in constructive architecture, single attractor is assessed and built upon and empirical study verification), and adding new hidden unit on top of previous learning architecture to embed learning new data. Due to these advantages, we developed NSL based on this cascading architecture for this task.

3. Edge computing system-ADC AIBot

ADC has successfully developed Low-cost Intelligent Security System (LISS) product and it is ready for the market. LISS is an intelligent edge computing system approach based on Raspberry Pi (3B and 4) and it is required no human attended. The report of the AIBot will be send to the user as specific time defined by the user and the complete app on Android is used to control whole network of the AIBots. It can work with almost all camera system as long as the interface is properly set up.

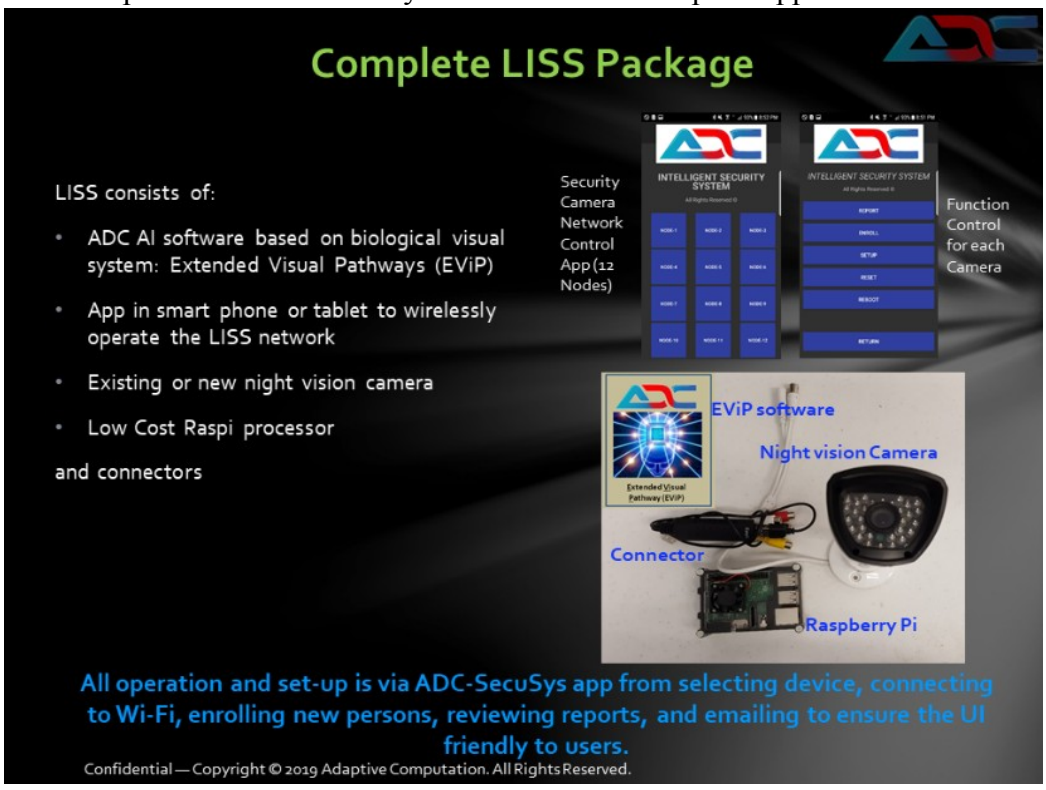

Figure 3: Live Intelligent and Unattended Face Recognition on Edge Raspberry Pi system

Low-cost Intelligent Security System (LISS): ***Ready for market***
LISS is a commercial product-ready package shown in Figure 3.

[7] T.A. Duong, "Cascade Error Projection-An efficient hardware learning algorithm," Proceeding Int'l IEEE/ICNN in Perth, Western Australia, vol. 1, pp. 175-178, Oct. 27-Dec 1, 1995.
[8] T.A. Duong, "*Cascade Error Projection Learning in Neural Network,"* Journal of NASA Tech Briefs, Vol. 25, No. 4, pp. 62, Apr 2001.

4. *Hybrid Intelligent Processing chip (HIP)*:
   A revolutionary hardware approach whose digitally-refined analog architecture[9] exploits "the best of both worlds" on a single chip, providing high speed, high performance, and low power consumption in a compact CMOS device. Using a unique combination of analog and digital circuit elements, the Hybrid Intelligent Processor (HIP) chip can serve as a high-speed correlator and self-adapting neural network processor. The development of this novel hybrid processing chip will enable powerful tools for edge, fog and central computing to tasking and information sharing to be incorporated directly into mobile devices or systems in limited SWAP environments. The **extremely small size and weight, and very low power requirement** of the HIP chip will make it ideal for use in unmanned aerial systems and other resource-limited applications.

The combination of the core technologies possessed by ADC is set a corner stone to tackle the challenges of BRIAR, to meet the IARPA's goals.

ADC Team

For this project, we have assembled a strong and diverse team including Dr. Tuan A Duong as PI, and Mr. Michael Lopez as DoD transition expert and Dr. Nam Trang as Data Science Lead. The PI is well-established in the image and pattern recognition field and he invented several learning algorithms based on introducing new objective functions for neural network and independent component analysis, to meet the application constraints. He also initiated extended visual pathway which consists of saccadic eye movement emulator and bio-inspired visual pathway to extract visual system with single sample data, on-line adaptive capability, to enable the machine intelligence. The DoD transition expert is an experienced and hand-on manager of technology transition to military. The Data Science Lead possesses an expert in data science. He has been the PI on several federally funded research grants and is currently awarded the NSF CAREER grant from the NSF Division of Mathematical Sciences.

Dr. Tuan A. Duong will serve as the Principal Investigator. His resume follows.

Tuan A. Duong is a CEO of Adaptive Computation LLC and had been a senior scientist in the Bio-inspired Technologies and Systems Group at the Jet Propulsion Laboratory/California Institute of Technology, Pasadena, California from 1995-2011. He received his Ph.D. from the University of California, Irvine, in electrical engineering. Tuan Duong's research focuses on technologies and systems related to image-based search engine, intelligent search, modeling and development of cognitive processing, artificial visual cortex computation and artificial nose e.g., Enose, chemical sensor (differential ion mobility spectrometry and 2-D spatial detector). He has been developing real time adaptive hybrid computing architectures to interface to and be capable of processing visual and olfactory sensors in real time. Moreover, this architecture will enable to process the fully parallel data streams from eyes and nose at different sampling rates. Parallel computing and adaptive processing are the fundamental building blocks of this technology. Significant contributions of his works include: 1) the successful development of image based search engine on desktop and Android based smart phone before Google announced its product;

[9] Tuan A. Duong, S. Kemeny, T. Daud, A. Thakoor, C. Saunders, and J. Carson, "*Analog 3-D Neuro-processor for Fast Frame Focal Plane Image Processing*," *The Industrial Electronics Handbook,* Chap. 73, Ed.-In-Chief J. David Irwin, CRC PRESS, 1997.

2) the effective mapping from visual pathway to solve real time moving object recognition; 3) the effective modeling to enable the Caltech and JPL Enose sensor project to extend the operation from homogeneous to heterogeneous environment for NASA's space applications.

For his invention of on-chip processing to improve the cost of NASA missions, he received the *2002 Exceptional NASA Space Act Award* for the creative development of exceptional scientific and technical contribution for aerospace technology program of NASA. He also received in *2004,* 2006 and 2009 Standard NASA Space Act Awards and received 30 NASA Technical Innovation and monetary awards, 12 patents and monetary awards (Caltech and NASA are assignees), 3 US and one international patents (ADC) and five provisional patents. He has published 115 papers and new technology reports and 3 book chapters.

He was an invitee to participate in Complex Systems Conference-08 in Irvine, California, Nov 13-15, 2008 and has been selected to participate in a group concept mapping project, 2014 in National Academies Keck Futures Initiative (NAKFI), a program of the National Academy of Sciences (NAS), the National Academy of Engineering (NAE), and the Institute of Medicine (IOM).

Selected Publications by the Principal Investigator:

1. US provisional patent, "High Speed, Low Power Search Engine Based on Hybrid and Digital Approach," T. A. Duong, ADC File No.: ADC-0003-P3, A# 62582595 Filed: 11/07/2017 **(ADC Assignee)**.
2. US patent, "*Artificial Intelligence Systems for Identifying Objects,"* T. A. Duong, V. A. Duong and Allen R. Stubberud, Patent Number: 7,711,157 Issued: 5/4/2010 **(Caltech Assignee)**.
3. US Patent, "*Method and System for Object Recognition Search*," T. A. Duong, V. A. Duong and A. R. Stubberud, Patent No. 8340435, Issue Date Dec. 25, 2012 **(Caltech Assignee)**.
4. US patent, " *Compressive Sensing based Bio-Inspired Shape Feature Detection CMOS Imager,*" T. A. Duong, Patent No. 8,976,269, Issue Date March 10, 2015 **(Caltech Assignee)**. T. A. Duong, "Real-Time Adaptive Color Segmentation by Neural Networks," Journal of NASA Tech Briefs, pp. 65, Nov 01, 2004.
5. T. A. Duong, "Real Time Adaptive Color Segmentation for Mars Landing Site Identification," Journal of Advanced Computational Intelligence and Intelligent Informatics, pp.289-293, Vol.7 No.3, 2003.
6. Tuan A. Duong, Vu A. Duong and Allen R. Stubberud, "*Shape and Color Features for Object Recognition Search,*" Handbook of Pattern Recognition and Computer Vision, Chap. 1.5, Ed. C.H. Chen, 4th Edition by World Scientific Publishing Co. Pte. Ltd, Jan 2010.
7. Tuan A. Duong, S. Kemeny, T. Daud, A. Thakoor, C. Saunders, and J. Carson, "*Analog 3-D Neuro-processor for Fast Frame Focal Plane Image Processing*," *The Industrial Electronics Handbook,* Chap. 73, Ed.-In-Chief J. David Irwin, CRC PRESS, 1997.
8. Tuan A. Duong, S.P. Eberhardt, T. Daud, and A. Thakoor, "*Learning in neural networks: VLSI implementation strategies*," In*: Fuzzy logic and Neural Network Handbook*, Chap. 27, Ed: C.H. Chen, McGraw-Hill, 1996.